

## **REMARKS**

This is a response to the Office Action mailed January 11, 2006. The Office Action noted the allowance of claims 1-6, 8, 9, 11, 15, 28-30, 41-43, and 45, rejected claims 35 under 35 U.S.C. §102, and rejected claims 20, 23, 24, 37, 39, 40, 44, and 46 under 35 U.S.C. §103.

Claims 20, 35, 37 have been amended, cancelled claims 44, 45 and 46, and added claims 47-49. Claims 1-6, 8-9, 11, 15, 20, 23, 24, 28, 29, 30, 35, 37, 39-43, 45, and 47-48 remain pending in this application.

Reconsideration in light of the amendments and remarks made herein is respectfully requested.

### **Rejections Under 35 U.S.C. § 102**

The Office Action rejected claims 35 under 35 U.S.C. §102(e) as being anticipated by Hosomi (U.S. Pat. No. 6,740,981).

To more clearly claim that which Applicants consider a novel aspect of the invention, claim 35 has been amended to recite “a stack of substrates”, “a memory device on each substrate”, and “five sides of the memory device are completely exposed and a sixth side of the memory device is partially exposed for improved heat dissipation.”

Applicants submit that Hosomi fails to teach that “five sides of the memory device are completely exposed and a sixth side of the memory device is partially exposed” as claimed. In particular, Hosomi (Figure 5) teaches that protective resin 60 is used to seal surfaces of the memory device 57.

As a result of these amendments, Applicants submit that independent claims 35 and its dependent claims are in condition of allowance.

### **Rejections Under 35 U.S.C. § 103**

The Office Action rejected claims 20, 37, 39, 40, 44, and 46 under 35 U.S.C. §103(a) as being unpatentable over Hosomi in view of Lo (U.S. Pat No. 5,953,210).

As to independent claims 20, 37, and 39, Applicants submit that there is no motivation to combine the cited features of Hosomi and Lo. As to these three independent claims, the Office Action asserts that Hosomi teaches the claimed stack and the lack of underfill for the semiconductor devices.

The Office has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1471-72 (Fed. Cir. 1984).

“Most, if not all, inventions are combinations of mostly old elements.” *Richdel, Inc., v. Sunspool Corp.*, 699 F.2d 1366 (Fed. Cir. 1983). “An Examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negation patentability, very few patents would ever issue.” *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998). “The legal conclusion of obviousness requires that there be some suggestion, motivation, or teaching in the prior art whereby the person of ordinary skill would have selected the components that the inventor selected and used them to make the new device.” *C.R. Bard, Inc. v. M3 Systems, Inc.*, 157 F.3d 1340 (Fed. Cir. 1998).

Assuming, arguendo, that Hosomi and Lo teach the claimed features, there is no motivation to combine their teachings. In fact, the motivation of Lo to remove the underfill from

the semiconductors is inconsistent with the physical configuration of the stack assembly taught by Hosomi.

Hosomi teaches a plurality of semiconductor devices modules stacked together to form a semiconductor module. (See Abstract) Each semiconductor device includes a substrate 50 and a semiconductor chip 57 mounted on the substrate, where a plurality of bumps 59 couple the semiconductor devices to each other to form a stack. A protective epoxy 60 is deposited on a plurality of surfaces of the semiconductor chip 57.

Lo teaches a flip chip 40 bonded to a circuit board 30 without using underfill or with a weak-bond strength underfill to facilitate removal of the flip chip 40 in the event of rework. (See Abstract) Lo does away with underfill to facilitate replacement of a failed chip on a multi-chip circuit board (Figure 3).

The Office Action states that “it would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the underfill or protective resin film from the memory devices of Hosomi as taught by Lo to provide an easy removal in the even of failure.” (Page 6) Applicants submit that combining Hosomi and Lo is contrary to their teachings. In particular, the reason Lo does not use underfill is that the invention relates to a single circuit board (Fig. 3) having multiple chips on one substrate which can be easily accessed for replacement. However, Hosomi teaches a stacked assembly in which multiple substrates are coupled to each other using a plurality of bumps. There is no motivation to omit the underfill in stacked device of Hosomi since it would not facilitate removal of failed memory devices. Unlike the semiconductor device 40 (Fig. 3) of Lo that lie on a single substrate 30 and can be easily accessed for removal, the semiconductor devices 57 of Hosomi are not easily accessed or

removed because they are tightly stacked with a plurality of bumps. Thus, unlike the easily removable semiconductor devices 40 of Lo, the bumps and stack configuration of Hosomi effectively prevent removal of the semiconductors 57 therein. Thus, the motivation to omit underfill provided by the Office Action (to facilitate removal of failed semiconductors) is contrary to physical limitations of the stacked assembly of Hosomi. There simply is no motivation to omit the underfill from the stacked semiconductor devices for ease of replacement (as asserted in the Office Action) since the bumps and tightly stacked configuration effectively prevent replacement of the semiconductor devices. Furthermore, no other motivation is disclosed in the Office Action or the cited prior art.

In the prior art, underfill has been used to improve the mechanical reliability between components (e.g., semiconductor die, die substrate, and module circuit board) having different coefficients of expansion to reduce the stresses operating on solder balls between these components. In the present application, Applicants are able to omit underfill between the semiconductor die, die substrate, and module substrate by selecting a die substrate that has a coefficient of thermal expansion (CTE) value in between the CTE values for the semiconductor die and the module substrate. This effectively balances out the thermal stresses of electrical joints between the die and die substrate interface and the thermal stresses between the die substrate and module substrate interface. Additionally, by omitting underfill from these interfaces, Applicants also lower the cost of manufacturing these modules and are able to improve heat dissipation of the dies.

Thus, as to claims 20 and 39, both of which substantively claim a main substrate with stacked chip-scale packages having a plurality of dies and die substrates, the prior art of Hosomi and Lo fail to teach balancing of CTE values of these three components to balance the stresses

perceived at these interfaces. It is by this balancing of CTE values that Applicants are able to improve reliability and omit underfill from each of these solder ball interfaces. To more explicitly claim this feature, Applicants have added dependent claims 47, 48 and 49.

Additionally, Applicants also submit that claim 20 includes the limitations (1) ‘a stack of memory devices’, (2) ‘the substrate having a coefficient of expansion that matches the coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less’, and (3) ‘a staggered routing scheme in a stacked semiconductor package.’ As noted in the Office Action, while these limitations are found in the cited prior art references, there is no motivation to combine them and, thus, their combination is allowable subject matter.

Applicants submit that as a result of the amendment made to independent claims 20, 37, and 39 and the remarks distinguishing the prior art, the remaining dependent claims are in condition for allowance.

#### **Allowable subject Matter**

Applicants note with appreciation the Examiner’s indication of allowable subject matter in claims 1-6, 8, 9, 11, 15, 28-30, 41-43, and 45.

### CONCLUSION

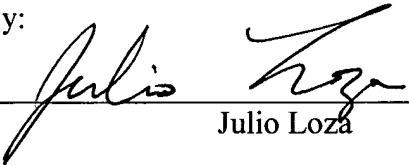
In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited. If an extension is required, then Applicants hereby request such an extension.

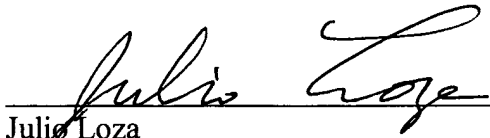
Respectfully submitted,

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I hereby certify that this document is being deposited on April 11, 2006 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313

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